

|   |  |   |  |
|---|--|---|--|
| FORM PTO 1390<br>(REV 10-2000)  |  | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | ATTORNEY'S DOCKET NUMBER<br>SIEBE96517-US  |
| TRANSMITTAL LETTER TO THE UNITED STATES<br>DESIGNATED/ELECTED OFFICE (DO/EO/US)<br>CONCERNING A FILING UNDER 35 U.S.C. 371  |  |   | U.S. APPLICATION NO. (If known, enter 37 CFR 1.5)<br>09/913859<br>To be assigned |
| INTERNATIONAL APPLICATION NO.<br>PCT/US00/04152   | INTERNATIONAL FILING DATES<br>18 February 2000 | PRIORITY DATE CLAIMED<br>18 February 1999               |  |
| TITLE OF INVENTION<br>Transformerless Power Supply, Dual Positive or Dual Negative Supplies   |  |   |  |
| APPLICANT(S) FOR DO/EO/US<br>Gregory J. Momber  |  |   |  |
| Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:   |  |   |  |
| <ol style="list-style-type: none"> <li>1. <input checked="" type="checkbox"/> This is a <b>FIRST</b> submission of items concerning a filing under 35 U.S.C. 371.</li> <li>2. <input type="checkbox"/> This is a <b>SECOND</b> or <b>SUBSEQUENT</b> submission of items concerning a filing under 35 U.S.C. 371.</li> <li>3. <input type="checkbox"/> This is an express request to promptly begin national examination procedures (35 U.S.C. 371 (f)).</li> <li>4. <input checked="" type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).</li> <li>5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371 (c)(2)) <ol style="list-style-type: none"> <li>a. <input type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau).</li> <li>b. <input type="checkbox"/> has been communicated by the International Bureau.</li> <li>c. <input checked="" type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US).</li> </ol> </li> <li>6. <input type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)).</li> <li>7. <input checked="" type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3)) <ol style="list-style-type: none"> <li>a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau).</li> <li>b. <input type="checkbox"/> have been communicated by the International Bureau.</li> <li>c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired.</li> <li>d. <input checked="" type="checkbox"/> have not been made and will not be made.</li> </ol> </li> <li>8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).</li> <li>9. <input type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).</li> <li>10. <input type="checkbox"/> An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).</li> </ol> |  |   |  |
| Items 11 to 16 below concern document(s) or information included:   |  |   |  |
| <ol style="list-style-type: none"> <li>11. <input type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98.</li> <li>12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 &amp; 3.31 is included.</li> <li>13. <input type="checkbox"/> A <b>FIRST</b> preliminary amendment.<br/><input type="checkbox"/> A <b>SECOND</b> or <b>SUBSEQUENT</b> preliminary amendment.</li> <li>14. <input type="checkbox"/> A substitute specification.</li> <li>15. <input type="checkbox"/> A change of power of attorney and/or address letter.</li> <li>16. <input checked="" type="checkbox"/> Other items or information: Two (2) Return Postcards.</li> </ol>   |  |   |  |

RECEIVED - 6 FEB 2000

|   |  |   |
|---|--|---|
| U.S. APPLICATION NO. (If known, see 37 CFR 1.5)<br><b>09/913859</b><br>To be assigned | INTERNATIONAL APPLICATION NO<br>PCT/US00/04152 | ATTORNEY'S DOCKET NUMBER<br>SIEBE96517-US |
|---|--|---|

| 17. <input checked="" type="checkbox"/> The following fees are submitted:<br><b>BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):</b><br><input type="checkbox"/> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO<br>And International Search Report not prepared by the EPO or JPO ..... \$1000.00<br><input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO ..... \$860.00<br><input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... \$710.00<br><input checked="" type="checkbox"/> International preliminary examination fee paid to USPTO (37 CFR 1.482)<br>But all claims did not satisfy provisions of PCT Article 33(1)-(4) ..... \$690.00<br><input type="checkbox"/> International preliminary examination fee paid to USPTO (37 CFR 1.482)<br>And all claims satisfied provisions of PCT Article 33(1)-(4) ..... \$100.00<br><br><div style="text-align: right;"><b>ENTER APPROPRIATE BASIC FEE AMOUNT =</b></div> <div style="text-align: right;">\$ 690.00</div><br>Surcharge of \$ 130.00 for furnishing the oath or declaration later than<br><input type="checkbox"/> 20 <input checked="" type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).<br><div style="text-align: right;">\$ 130.00</div><br><table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">CLAIMS</th> <th style="width: 20%;">NUMBER FILED</th> <th style="width: 20%;">NUMBER EXTRA</th> <th style="width: 20%;">RATE</th> <th style="width: 20%;"></th> </tr> </thead> <tbody> <tr> <td>Total claims</td> <td>25 - 20 =</td> <td>5</td> <td>x 18</td> <td>\$ 90.00</td> </tr> <tr> <td>Independent claims</td> <td>4 - 3</td> <td>1</td> <td>x 80</td> <td>\$ 80.00</td> </tr> <tr> <td colspan="4">MULTIPLE DEPENDENT CLAIM(s) (if applicable)</td> <td>\$</td> </tr> <tr> <td colspan="4"><b>TOTAL OF ABOVE CALCULATIONS =</b></td> <td>\$</td> </tr> <tr> <td colspan="4"> <input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above<br/>           Are reduced by 1/2.         </td> <td>\$</td> </tr> <tr> <td colspan="4"><b>SUBTOTAL =</b></td> <td>\$</td> </tr> <tr> <td colspan="4">           Processing fee of \$ _____ for furnishing the English translation later than<br/> <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +         </td> <td>\$</td> </tr> <tr> <td colspan="4"><b>TOTAL NATIONAL FEE =</b></td> <td>\$ 990.00</td> </tr> <tr> <td colspan="4">           Fee for recording the enclosed assignment (37 CFR 1.21 (h)). Assignment<br/>           must be accompanied by appropriate cover sheet (37 CFR 3.28, 3.31)<br/>           ( _____ per property). +         </td> <td>\$</td> </tr> <tr> <td colspan="4"><b>TOTAL FEES ENCLOSED =</b></td> <td>\$ 990.00</td> </tr> <tr> <td colspan="4"></td> <td style="text-align: right;">Amount to be Refunded: \$</td> </tr> <tr> <td colspan="4"></td> <td style="text-align: right;">Charged: \$</td> </tr> </tbody></table> | CLAIMS       | NUMBER FILED | NUMBER EXTRA | RATE                      |  | Total claims | 25 - 20 = | 5 | x 18 | \$ 90.00 | Independent claims | 4 - 3 | 1 | x 80 | \$ 80.00 | MULTIPLE DEPENDENT CLAIM(s) (if applicable) |  |  |  | \$ | <b>TOTAL OF ABOVE CALCULATIONS =</b> |  |  |  | \$ | <input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above<br>Are reduced by 1/2. |  |  |  | \$ | <b>SUBTOTAL =</b> |  |  |  | \$ | Processing fee of \$ _____ for furnishing the English translation later than<br><input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). + |  |  |  | \$ | <b>TOTAL NATIONAL FEE =</b> |  |  |  | \$ 990.00 | Fee for recording the enclosed assignment (37 CFR 1.21 (h)). Assignment<br>must be accompanied by appropriate cover sheet (37 CFR 3.28, 3.31)<br>( _____ per property). + |  |  |  | \$ | <b>TOTAL FEES ENCLOSED =</b> |  |  |  | \$ 990.00 |  |  |  |  | Amount to be Refunded: \$ |  |  |  |  | Charged: \$ | <b>CALCULATIONS PTO USE ONLY</b> |
|--|--------------|--------------|--------------|---------------------------|--|--------------|-----------|---|------|----------|--------------------|-------|---|------|----------|---|--|--|--|----|--------------------------------------|--|--|--|----|---|--|--|--|----|-------------------|--|--|--|----|--|--|--|--|----|-----------------------------|--|--|--|-----------|---|--|--|--|----|------------------------------|--|--|--|-----------|--|--|--|--|---------------------------|--|--|--|--|-------------|----------------------------------|
| CLAIMS   | NUMBER FILED | NUMBER EXTRA | RATE         |                           |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| Total claims   | 25 - 20 =    | 5            | x 18         | \$ 90.00                  |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| Independent claims   | 4 - 3        | 1            | x 80         | \$ 80.00                  |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| MULTIPLE DEPENDENT CLAIM(s) (if applicable)  |              |              |              | \$                        |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| <b>TOTAL OF ABOVE CALCULATIONS =</b>   |              |              |              | \$                        |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| <input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above<br>Are reduced by 1/2.  |              |              |              | \$                        |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| <b>SUBTOTAL =</b>  |              |              |              | \$                        |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| Processing fee of \$ _____ for furnishing the English translation later than<br><input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +   |              |              |              | \$                        |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| <b>TOTAL NATIONAL FEE =</b>  |              |              |              | \$ 990.00                 |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| Fee for recording the enclosed assignment (37 CFR 1.21 (h)). Assignment<br>must be accompanied by appropriate cover sheet (37 CFR 3.28, 3.31)<br>( _____ per property). +  |              |              |              | \$                        |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
| <b>TOTAL FEES ENCLOSED =</b>   |              |              |              | \$ 990.00                 |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
|  |              |              |              | Amount to be Refunded: \$ |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |
|  |              |              |              | Charged: \$               |  |              |           |   |      |          |                    |       |   |      |          |   |  |  |  |    |                                      |  |  |  |    |   |  |  |  |    |                   |  |  |  |    |  |  |  |  |    |                             |  |  |  |           |   |  |  |  |    |                              |  |  |  |           |  |  |  |  |                           |  |  |  |  |             |                                  |

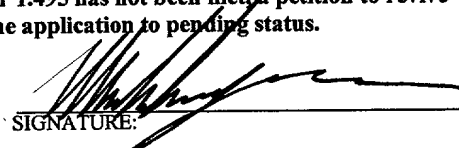
a. ☒ A check in the amount of \$ 990.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. \_\_\_\_\_ in the amount of \$ \_\_\_\_\_  
 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required or credit  
 any overpayment to my Deposit Account No. 06-2375. A duplicate copy of this sheet is enclosed.

**NOTE:** Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive  
 (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

  
 SIGNATURE:

Mark Ungerman  
 NAME

32,070  
 REGISTRATION NUMBER

RECEIVED - 08/20/01

**TRANSFORMERLESS POWER SUPPLY, DUAL POSITIVE  
 OR DUAL NEGATIVE SUPPLIES**

**BACKGROUND OF THE INVENTION**

5

**1. Field of the Invention**

The present invention relates to a transformerless direct current (dc) power supply. More particularly, this invention is directed to a circuit for being interconnected to a high voltage alternating current (ac) supply producing either a dual positive or a dual negative dc power supply.

10

**2. Description of the Related Technology**

Transformerless capacitor arrangements for creating a low voltage direct current source are well known in the field of power supplies. One simple example is the half-wave voltage doubler consisting of two diodes and two capacitors. The circuit is shown in FIG. 7, along with its voltage source, load resistance and voltage regulator.

15

The operation of the half-wave doubler is easy to understand. During the negative alterations of the ac input, diode (126) is reversed biased and diode (127) is forward biased by the ac input signal polarity. Capacitor (143) is charged until its plate-to-plate voltage is equal to the source voltage. At the same time, capacitor (144) is discharging through the load resistance.

20

When the ac input polarity reverses, diode (127) is off. Capacitor (143) is charged to the peak value of  $V_{L1(PK)}$  and the source voltage now acts as a series-aiding source. Thus, capacitor (144) is charged to the sum of the series of the peak voltages,  $2 V_{L1(PK)}$ .

25

When  $V_s$  returns to its original polarity, diode (126) is again turned off. Once diode (126) is off, the only charge path for capacitor (144) is through the load resistance. Normally, the time constant of this current circuit will be such that capacitor (144) has little time to lose any of its charge before the input reverses polarity again. In other words, during the negative

000000-000000

alteration of the input, capacitor (144) will be discharged slightly. Then, during the positive alterations, diode (126) is turned on and capacitor (144) recharges until its plate-to-plate voltage again equals  $2V_{L1(PK)}$ .

Since capacitor (144) barely discharged between input cycles, the output wave-form of the half-wave voltage doubler closely resembles that of a filtered half-wave rectifier. Typical input and output waveforms for a half-wave voltage doubler are shown in FIG. 6. As the figure shows, the circuit will have a dc output voltage and a ripple voltage that closely resembles the output from a filtered rectifier. The dc output voltage is approximated as

$$V_{dc} \approx 2 V_{L1(PK)}$$

The output ripple voltage is calculated using the same process that was used for the filtered half-wave rectifier.

$$V_r \approx \frac{I_L t}{C}$$

where  $V_r$  = ripple voltage peak-to-peak  
 $I_L$  = dc load current  
 $t$  = time between charging peaks  
 $C$  = capacitance

Incidentally, if the directions of diodes 126 and 127 are reversed, the result is a negative half-wave voltage doubler.

One application for the voltage multiplier can be seen in a basic dual-polarity dc power supply. A dual-polarity supply is one that provides both a positive and a negative dc output voltage. One such supply is shown in FIG. 8. Thus, point A will be positive with respect to ground and point B will be negative with respect to ground. Note that the two dc output voltages will be approximately equal to the magnitude of  $V_{L1(PK)}$ . For example, if  $V_{L1(PK)}$  is 24 V<sub>pk</sub>, the power supply will have outputs that are approximately equal to +24 V<sub>dc</sub> and -24 V<sub>dc</sub>. Conventional transformerless capacitor arrangements produce one negative and one positive supply thus requiring more energy. These supplies are exemplified in U.S. Patent No.

5,440,443 and U.S. Patent No. 5,365,146, the disclosures of which are incorporated herein by reference. It is the Applicant's belief that the prior art has not used a transformerless capacitor arrangement for converting either the positive or negative supply to the opposite polarity.

5

### SUMMARY OF THE INVENTION

The present invention provides a dual positive or a dual negative output power supply instead of the traditional one positive and one negative output supply. The direct current (dc) power supply unit has a transformerless capacitor arrangement for creating a first low voltage dc output and a second low voltage dc output from an alternating current (ac) power supply wherein the second dc output has the same plurality of the first dc output. Inverting the polarity is accomplished by a transistor in either the common emitter configuration or the common source configuration.

10

In another embodiment, a relay voltage may be provided that may be controlled by a microprocessor.

15

An object of the invention is to provide a circuit that delivers two positive or two negative power supply voltages as opposed to the single negative and single positive power supply previously disclosed.

It is an object of the present invention to cost effectively simulate the power generated from a full wave rectifier circuit.

20

It is an object of the present invention to provide a low power source for electronic controls.

It is an object of the present invention to provide a safety feature for a power supply.

### BRIEF DESCRIPTION OF THE DRAWINGS

25

FIG. 1 shows the details of the circuit during the positive-half line cycle.

FIG. 2 shows the details of the circuit during the negative-half line cycle.

FIG. 3 shows the details of the circuit during the positive-half when capacitor voltage reaches the zener threshold.

FIG. 4 shows the details of the circuit during the negative-half when capacitor voltage reaches the zener threshold.

FIG. 5A shows a dual negative supply.

FIG. 5B shows a dual positive supply.

5 FIG. 5C shows an alternate dual negative supply.

FIG. 5D shows an alternate dual positive supply.

FIG. 6 shows typical input and output waveforms for a half-wave voltage doubler.

FIG. 7 shows a prior art power supply.

FIG. 8 shows a prior art dual power supply.

10 FIG. 9 shows another embodiment of the invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

15 A power supply can be broken down into three circuit groups: rectifier, filter and voltage regulator. In the first group, an alternating current (ac) input signal is applied to a rectifier circuit for converting the ac input signal into a pulsating direct signal (dc) output signal. This pulsating dc output signal is then applied to a filter circuit to reduce the variations in the dc voltage. The final stage is the voltage regulator circuit which is used to maintain a constant output signal.

20 According to an advantageous feature of the invention, an ac input signal may be applied to a first wave rectifier for a positive-half cycle of the ac input signal to produce a pulsating dc output signal. The output signal of the first wave rectifier may then be applied to a first filter and a first voltage regulator (e.g., one zener diode or two series zener diodes) to produce a first power supply. During the negative-half cycle of the ac input signal, a transistor in either a common emitter or common source configuration may be used to shift the ac input  
25 signal by 180 degrees. This shifted voltage is then applied to a second rectifier for converting the shifted ac input signal into a pulsating dc output signal. The shifted pulsating dc output signal is applied to a second filter to reduce the variations in the signal. Finally, the output of the second filter is applied to a second voltage regulator (e.g., one zener diode or two series

zener diodes) to produce a second power supply. The second power supply will have the same polarity as the first power supply.

FIG. 5A shows the operation of the above embodiment. FIGS. 1-4 break down the operation of FIG. 5A into half cycles of the input ac input signal (*i.e.*, positive-half cycle and negative-half cycle). FIGS. 1-4 only show the active components of the circuit during the particular half cycle.

FIG. 1 shows the positive-half of an ac input signal during the first few cycles of the ac input signal (*i.e.*, when the voltage at  $L_1$  (1) is positive). On the positive-half cycle, diode (20) will conduct current that flows through capacitor (41), diode (22), resistor (11), and then back to neutral (2). The voltage that is developed across capacitor (41) (approximately 7 v/step in this case) is a function of the value of capacitor (40) and capacitor (41) and the number of iterations (each cycle) that this process undergoes. For the first few cycles of the ac input signal, zener diodes (30 and 31) are not active components in the circuit and only become active after the capacitor voltage reaches the zener threshold as seen in FIG. 3. Furthermore, during the positive-half cycle of the ac input signal, transistor (50) will be in the off state.

FIG. 2 shows the active components of the embodiment when the voltage at  $L_1$  (1) is negative. During the negative-half cycle of the ac input signal, diode (23) may conduct current that flows into capacitor (43), through resistor (11) and then back to neutral (2). The voltage that is developed across capacitor (43) (approximately 1.5 v/step in this case) is a function of the values of capacitors (40 and 42) and the number of iterations that this process undergoes. For the first few cycles of the ac input signal, zener diodes (32 and 33) may not be active components in the circuit. As shown in FIG. 4, the zener diodes become active after the capacitor voltage reaches the zener threshold. The transistor (50) will be turned on as soon as the line voltage goes negative and when this occurs, capacitor (41) is then discharged into capacitor (42). The discharge path is: transistor (50) collector to emitter, to resistor (12), to capacitor (41), to diode (21), and to capacitor (42). This results in a voltage reversal at the anode of diode (21). This process will continue until the voltage on capacitor (42) is equal to the combined zener voltages of zener diode (30) and zener diode (31). The values of resistor

(13) and resistor (14) determine the actual voltage threshold for transistor (50), and resistor (12) is present to limit the collector current to some tolerable level. In FIG. 5A (for dual negative supplies) and FIG. 5B (dual positive supplies), transistor (50) is shown in the common emitter configuration. FIG. 5C (dual negative supplies) and 5D (dual positive supplies) show transistor (50) in the common source configuration.

The end result is the circuit may deliver two positive or two negative power supplies as opposed to the single negative and single positive power supply disclosed as prior art.

In another embodiment of the invention, a dual positive or dual negative power supply circuit may include a relay voltage ( $V_r$ ), which may be controlled by a microprocessor to provide a safety feature for an electronic device. The relay voltage may be used to power additional circuits, which require insulation from component faults. For example, the relay voltage may be used to power a gas valve. If the gas valve is unintendedly activated, a fire may inadvertently occur.

In FIG. 9, an embodiment of the invention is shown with dual positive power supplies. The component values shown in FIG. 9 are for illustrative purposes only and are not intended to limit the disclosure. Dual negative power supplies may be provided similar to the previous embodiments by simple component modifications.

FIG. 9 shows an embodiment of the invention that is similar to the embodiment shown in FIG. 5B with the exception of  $R_4$  and  $R_5$ . In FIG. 5B, during the negative-half cycle of the ac input signal,  $R_4$  and  $R_5$  appropriately cycled  $Q_1$  to develop voltage on  $C_3$ , in order to provide a second positive voltage supply, which may be the same polarity as the first supply voltage. In the embodiment of FIG. 9,  $R_4$  and  $R_5$  (FIG. 5B) may be replaced with a level shifter circuit including the following elements:  $R_5$ ,  $R_6$ ,  $R_7$ ,  $R_{47}$ ,  $Q_9$  AND  $Q_2$ . In addition, for safety,  $D_3$  and  $R_8$  may be added to provide a line synchronization to a microprocessor (not shown). This configuration allows a microprocessor to directly control this portion of the power supply. When the microprocessor controls this portion of the circuit, the power supply may be directly inhibited to prevent any voltage from building at relay supply voltage  $V_R$ . If the relay supply voltage is inhibited, a single component fault (e.g., shorted drive transistor connected to the



relay coil) will not cause the relay to activate without permission from the microprocessor. Furthermore, the relay voltage may be disabled by leaving  $Q_1$  continuously activated.

In FIG. 9, line voltage ( $L_1$ ) may be connected to reactive element  $C_1$ , (2.7  $\mu$ F 250V) to provide a voltage drop in the supply and to introduce a +90° current phase shift. Resistor  $R_{46}$  (1.0M $\Omega$  0.25W) may be connected in parallel with  $C_1$  to dissipate any charge remaining when power is removed.  $C_1/R_{46}$  may then be connected to current limiting resistors  $R_1$  and  $R_2$  (27 $\Omega$  1W each). Note that  $R_2$  is in series with neutral. This is followed by shunt capacitor  $C_{12}$  (0.047  $\mu$ F 100V) and series inductor  $L_1$  (560 $\mu$ H) for noise filtering. The filter's output may then be fed to rectifier diodes  $D_1$ ,  $D_2$ ,  $D_4$ , and  $D_5$  (1N4007 each), and is also sent to the line sync circuit.

Similar to the previous embodiments, during negative half-cycles of the ac input signal, the signal may be applied to the rectifier circuit, diodes  $D_2$  and  $D_4$ . The diodes conduct to charge filter capacitor  $C_5$  (100 $\mu$ F 63V). The voltage may be limited or regulated by a series string of zener diodes  $Z_3$ ,  $Z_4$ , and  $Z_5$  (18V 1N4746 each) connected across  $D_4$  and  $C_5$ . The output of the voltage regulator circuit,  $Z_3$ ,  $Z_4$ , and  $Z_5$ , may be a first dc output voltage exhibiting a first polarity.

During positive half-cycles of the input signal, diode  $D_1$  conducts to charge filter capacitor  $C_2$  (100 $\mu$ F 16V). The voltage across  $C_2$  may be clamped or regulated by a voltage regulator, shunt zener diode  $Z_1$  and  $Z_6$  (5.1V 1N4733A each). This node may then be fed through resistor  $R_3$  (22 $\Omega$  0.25W) to shunt zener diode  $Z_2$  (5.1V 1N5993), which results in a regulated 5 Vdc ( $V_{cc}$ ), a second dc output voltage with the same polarity as the first dc output voltage.  $V_{cc}$  may be used by the microprocessor and other related circuitry.

In this embodiment, a relay supply voltage ( $V_R$ ) may be established during positive half-cycles of the ac input signal by transferring a charge from capacitor  $C_5$  to  $C_4$  (470 $\mu$ F 63V) through diode  $D_3$  (1N4007) and resistor  $R_4$  (51 $\Omega$  0.25W). The circuit may be completed by turning on transistor  $Q_1$  (MPSA06) to provide a return path to  $C_5$ .  $Q_1$  may be controlled by a microprocessor (not shown) through the level shifter made up of transistors  $Q_2$  (2N2907) and  $Q_9$  (MPSA56) along with resistors  $R_5$  (1.5 $\Omega$  0.25W),  $R_6$  (47 $\Omega$  0.25W),  $R_{47}$  (47k $\Omega$  0.25W),  $R_{45}$  (470k $\Omega$  0.25W), and  $R_7$  (470k $\Omega$  0.25W). Furthermore, the relay voltage may be disabled by

The microprocessor may require synchronization with the incoming signal to properly  
5 operate the circuit. If the line synchronization is lost, the control will lock out. The line sync  
circuit generates a logic level square wave at line frequency. This signal may used by the  
microprocessor and other circuitry for synchronization.

The junction of R<sub>8</sub> and R<sub>9</sub> may be connected to the microprocessor, where input clamping diodes will limit the peak voltage to one diode drop above +5V. This voltage may also be fed to other circuitry.

I claim:

- 1 1. A dual output transformerless power supply comprising:
  - 2 a first dc output stage responsive to an ac input, having a first wave rectifier including
  - 3 at least one diode with a regulated dc output exhibiting a first polarity, and including a first
  - 4 voltage regulator having at least one zener diode; and
  - 5 a second dc output stage responsive to said ac input, having a second wave rectifier
  - 6 including at least one diode with a regulated dc output inverted to said first polarity, and
  - 7 including second voltage regulator having at least one zener diode.
- 1 2. A dual output transformerless power supply, according to claim 1, wherein said second dc
- 2 output stage further comprises:
  - 3 an inverter connected to said second wave rectifier.
- 1 3. A dual output transformerless power supply, according to claim 1, wherein said second dc
- 2 output stage further comprises:
  - 3 an inverter which includes a transistor connected to said second wave rectifier.
- 1 4. A dual output transformerless power supply, according to claim 1, wherein said second dc
- 2 output stage further comprises:
  - 3 an inverter which includes a transistor in a common emitter configuration connected
  - 4 to said second wave rectifier.

1        5. A dual output transformerless power supply, according to claim 1, wherein said second dc  
2        output stage further comprises:

3           an inverter which includes a transistor in a common source configuration connected to  
4   said second wave rectifier.

1 6. A dual output transformerless power supply, according to claim 1, further comprising:

2 a first capacitor connected to said first dc output stage; and

3 a second capacitor connected to said second dc output stage.

1      7. A dual output transformerless power supply, according to claim 1, wherein:

2        said first voltage regulator circuit is connected to said first wave rectifier; and

3        said second voltage regulator circuit is connected to said second wave rectifier.

1 8. A dual output transformerless power supply, according to claim 1, further comprising:

2        said first voltage regulator circuit connected to said first wave rectifier having one or  
3        more zener diodes in series connected to a first filter; and

4                said second voltage regulator circuit connected to said second wave rectifier having one  
5                or more zener diodes in series connected to a second filter.

- 1 9. A dual output transformerless power supply, according to claim 1, further comprising:  
2       said first voltage regulator circuit connected to said first wave rectifier having a first and  
3       second zener diode in series; and  
4       said second voltage regulator circuit connected to said second wave rectifier circuit  
5       having a first and second zener diode in series.
- 1 10. A dual output transformerless power supply, according to claim 1, further comprising:  
2       a first capacitor connected to the output of said first wave rectifier; and  
3       a second capacitor connected to the output of said second wave rectifier.
- 1 11. A dual output transformerless power supply, according to claim 1, further comprising:  
2       a relay voltage which is controlled by a microprocessor.
- 1 12. A dual output transformerless power supply, according to claim 11, wherein the  
2       microprocessor is controlled by a level shifter circuit.
- 1 13. A dual output transformerless power supply comprising:  
2       first means for rectifying an ac input generating a first dc output signal having a first  
3       polarity;  
4       second means for rectifying an ac input generating a second dc output signal having  
5       said first polarity.

- 1 14. A dual output transformerless power supply, according to claim 13, further comprising:  
2 means for inverting said second dc output signal.
- 1 15. A dual output transformerless power supply, according to claim 13, further comprising:  
2 means for shifting said ac input 180 degrees for input into said second means for  
3 rectifying.
- 1 16. A dual output transformerless power supply, according to claim 13, further comprising:  
2 first means for filtering said first dc output signal.
- 1 17. A dual output transformerless power supply, according to claim 13, further comprising:  
2 second means for filtering said second dc output signal.
- 1 18. A dual output transformerless power supply, according to claim 16, further comprising:  
2 second means for filtering said second dc output signal.
- 1 19. A dual output transformerless power supply, according to claim 13, further comprising:  
2 first means for voltage regulation of said first dc output signal.
- 1 20. A dual output transformerless power supply, according to claim 13, further comprising:  
2 second means for voltage regulation of said second dc output signal.

1 21. A dual output transformerless power supply, according to claim 19, further comprising:

2 second means for voltage regulation of said second dc output signal.

1 22. A dual output transformerless power supply comprising:

2 first means for rectifying an ac input generating a first dc output signal having a first  
3 polarity;

4 first means for filtering said first dc output signal connected to said first means for  
5 rectifying;

6 first means for voltage regulation connected to said means for filtering;

7 second means for rectifying an ac input generating a second dc output signal having  
8 said first polarity;

9 second means for filtering said second dc output signal connected to said second means  
10 for rectifying;

11 second means for voltage regulation connected to said second means for filtering;

12 means for inverting connected to said second means for voltage regulation.

1     23. A method for providing a dual output transformerless power supply comprising the steps

2 of:

3 converting an ac input signal during a first half-cycle to a first dc output with a first

4 polarity;

5 converting the ac input during a second half-cycle to a second dc output with the same

6 polarity as the first dc output.

1     24. A method for providing a dual output transformerless power supply, according to claim

2 23, further comprising the step of:

3 providing a relay voltage.

1 25. A method for providing a dual output transformerless power supply, according to claim

2 24, further comprising the step of:

3 controlling the relay voltage with a control circuit.

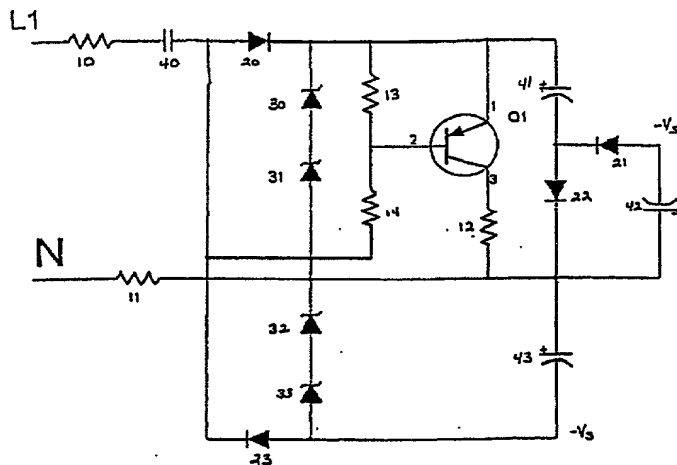




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

|  |  |   |
|--|--|---|
| (51) International Patent Classification 7 :<br>H02M 7/00, 5/42, 7/04, 7/63, 7/06, G05F<br>1/613, 3/00, 1/618  |  | (11) International Publication Number: <b>WO 00/49707</b>                                 |
| A1   |  | (43) International Publication Date: 24 August 2000 (24.08.00)                            |
| (21) International Application Number: PCT/US00/04152<br>(22) International Filing Date: 18 February 2000 (18.02.00)<br>(30) Priority Data:<br>60/120,586 18 February 1999 (18.02.99) US<br>(71) Applicant (for all designated States except US):<br>ROBERTSHAW CONTROLS COMPANY [US/US];<br>2809 Emerywood Parkway, Richmond, VA 23261-6544<br>(US).<br>(72) Inventor; and<br>(75) Inventor/Applicant (for US only): MOMBER, Gregory, J.<br>[US/US]; 7129 Peach Ridge Road, Grand Rapids, MI 49504<br>(US).<br>(74) Agents: MARTIN, Terrence; Invensys, Intellectual Property<br>Department, B52-1J, 33 Commercial Street, Foxboro, MA<br>02035 (US) et al. |  | (81) Designated States: CA, MX, US.<br><br>Published<br>With international search report. |

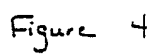
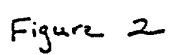
(54) Title: TRANSFORMLESS POWER SUPPLY, DUAL POSITIVE OR DUAL NEGATIVE SUPPLIES



## (57) Abstract

The positive half-cycle for an AC input signal is applied to wave rectifier (20, 22), a filter and a voltage regulator (30, 31) for generating a dc output signal. The ac input signal is also applied to a transistor (50) in either the common emitter or common source configuration which shifts the ac input signal by 180 degrees. This signal is then applied to another rectifier (21, 23) for converting the shifted ac input signal into a pulsating dc output signal. Then shifted dc output signal is applied to a second capacitor filter to reduce the signal variations. The final stage for the second output stage is also a voltage regulator (32, 33), i.e., two series zener diodes). The transformerless power supply produces either a dual positive or dual negative dc voltage supply. In addition, the voltage supply circuits may include a relay voltage, which may be controlled by a control circuit.



[illegible]

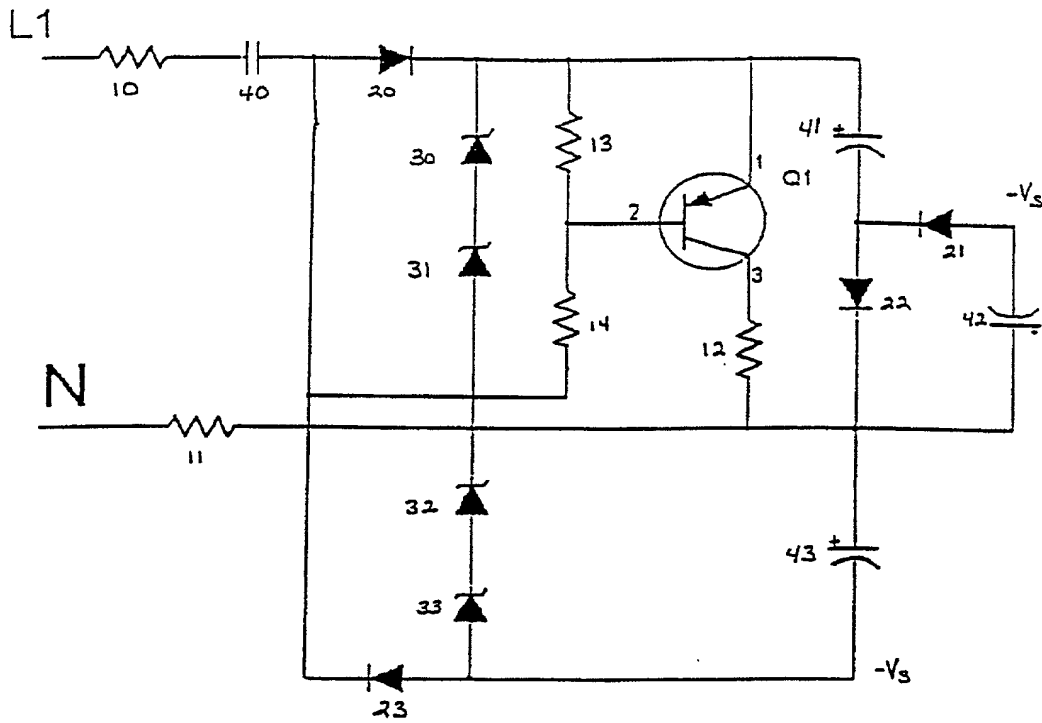


Figure 5a

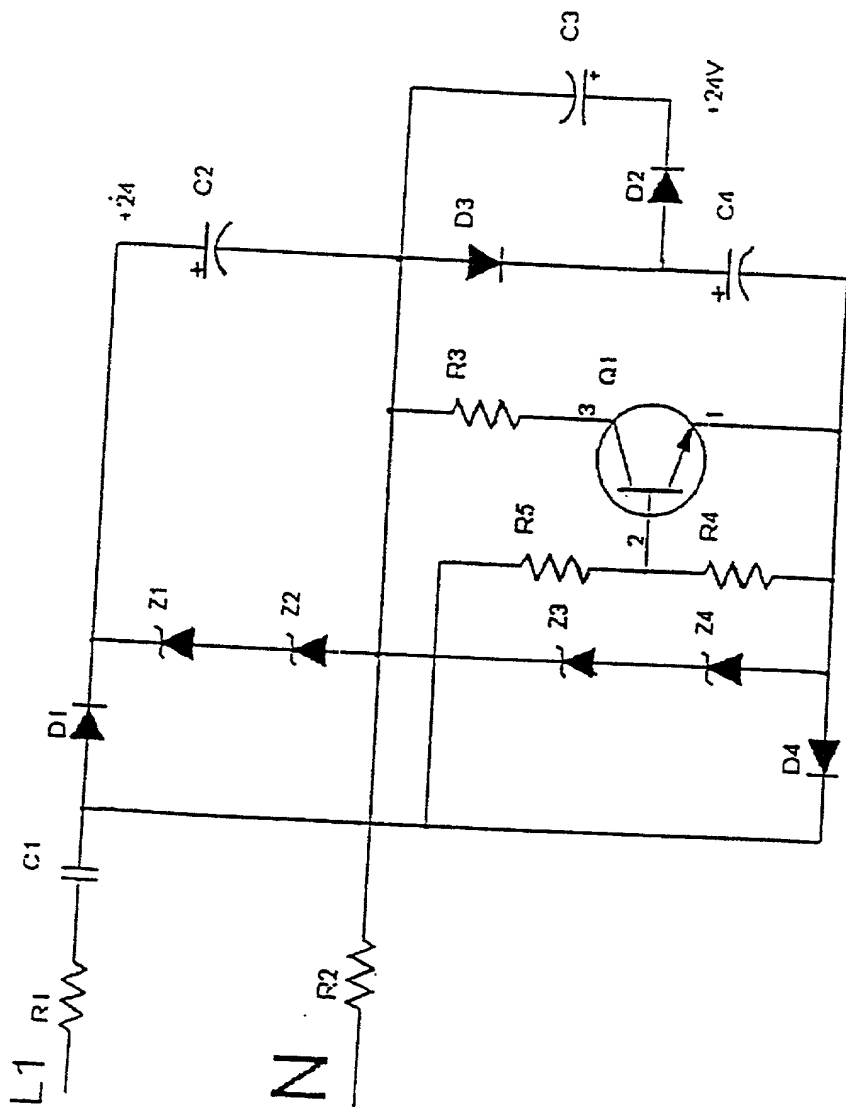


Figure 5b

09/913 859

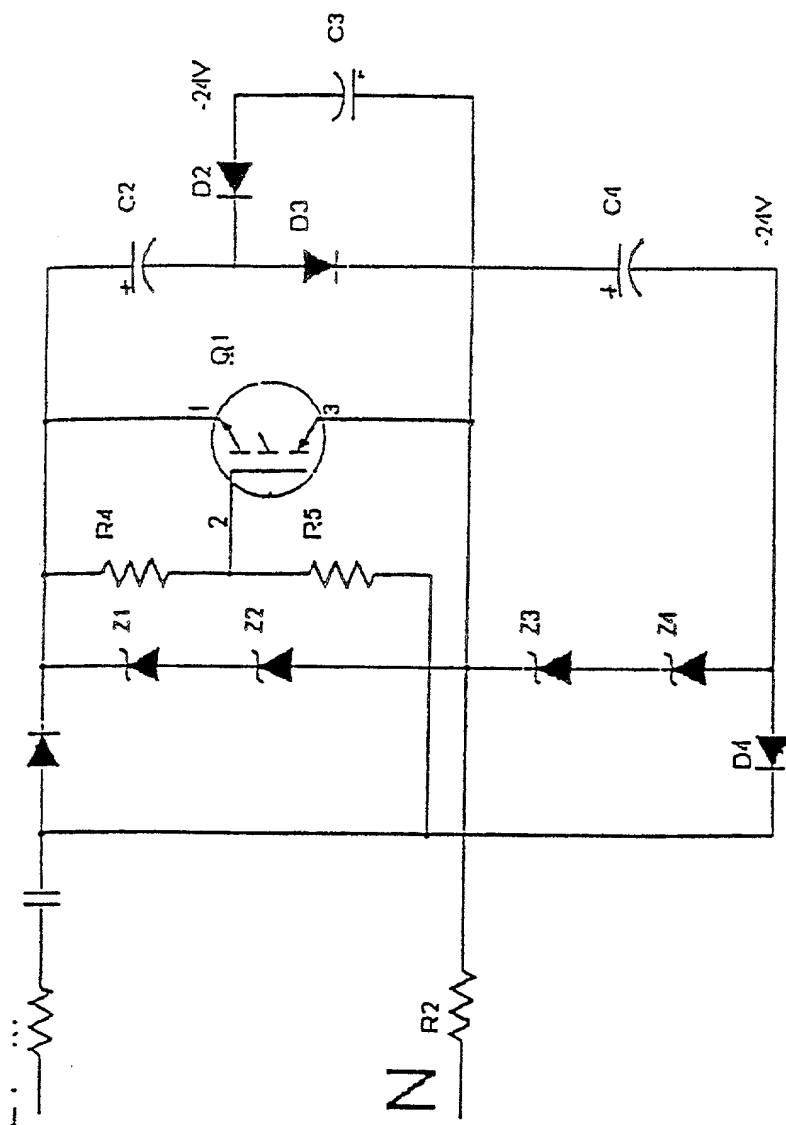


Figure 5c

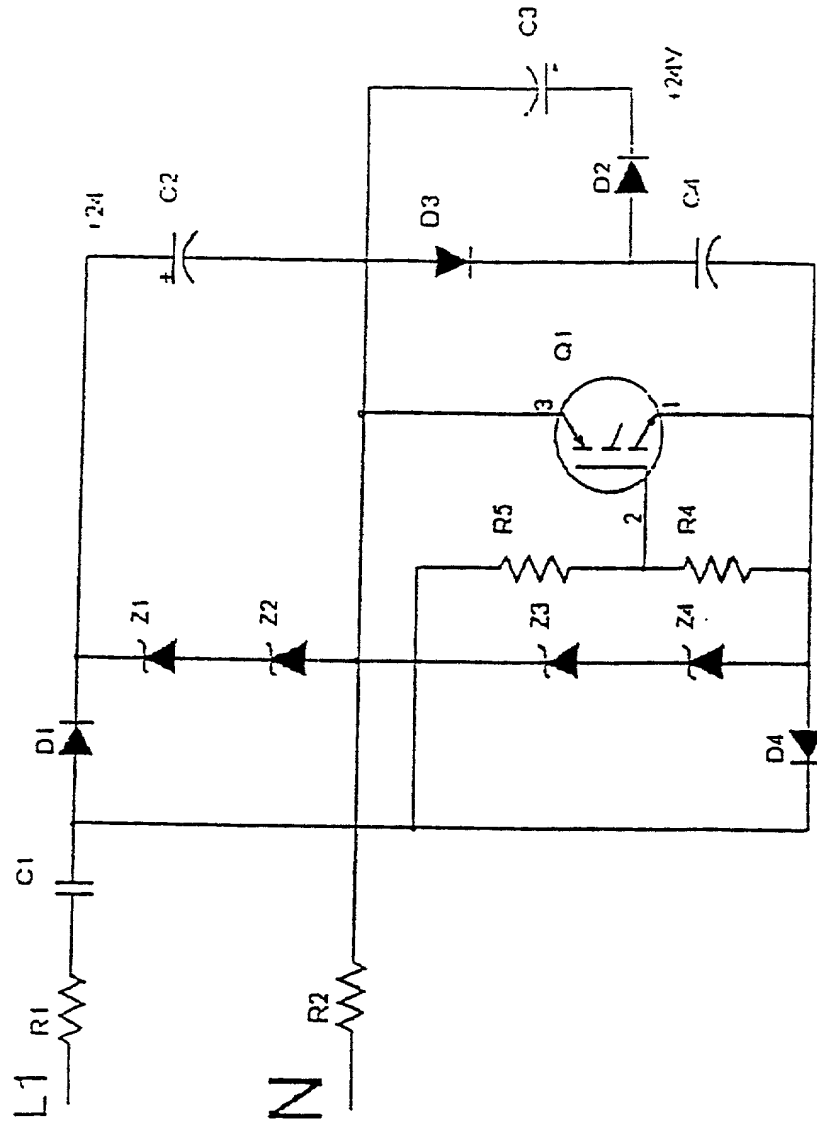


Figure 5 d

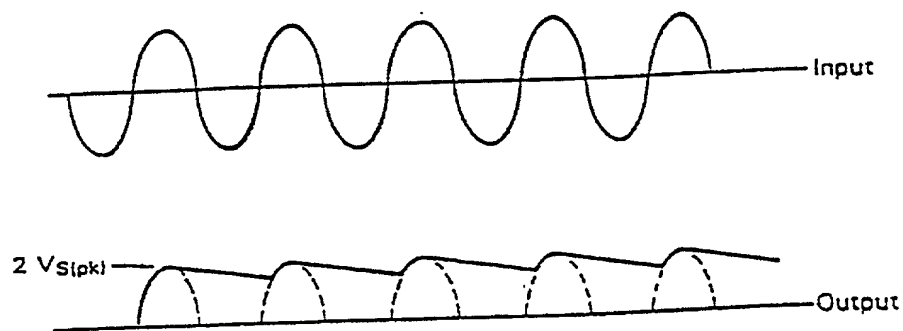


Figure 6



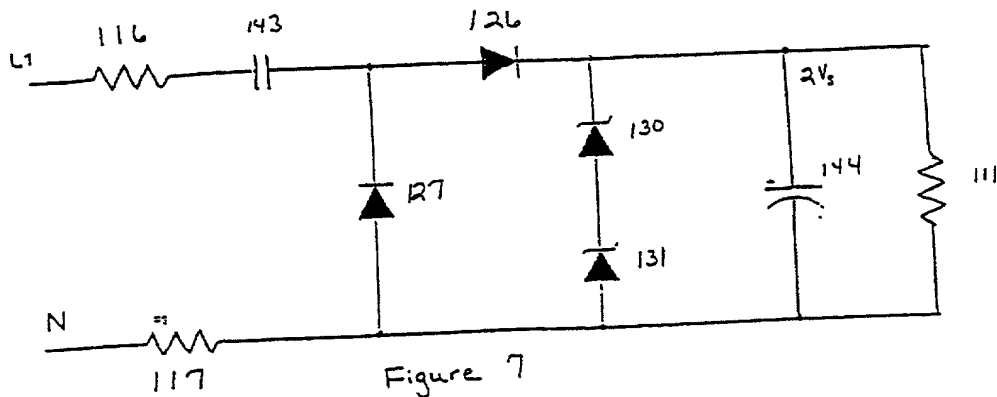


Figure 7  
PRIOR ART

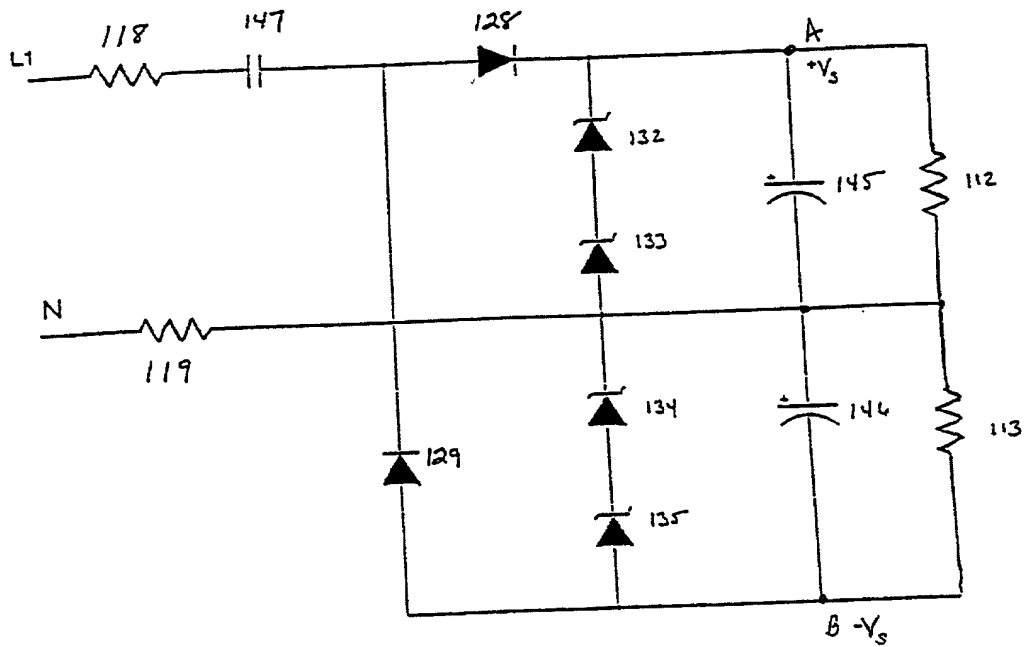


Figure 8  
PRIOR ART

**DECLARATION**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TRANSFORMERLESS POWER SUPPLY, DUAL POSITIVE OR DUAL NEGATIVE SUPPLIES

the specification of which [check one]

☐ is attached hereto

☒ was described and claimed in PCT International Application No. PCT/US00/004152 filed on August 5, 1999 and as amended under PCT Article 19 on \_\_\_\_\_ (if any).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

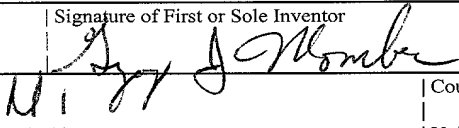
Priority Claimed

|                            |                    |   |   |                             |
|----------------------------|--------------------|---|---|-----------------------------|
| PCT/US00/04152<br>(Number) | PCT<br>(Country)   | 18 February 2000 (18/02/00)<br>(Day/Month/Year filed) | <input checked="" type="checkbox"/> Yes | <input type="checkbox"/> No |
| _____<br>(Number)          | _____<br>(Country) | _____<br>(Day/Month/Year filed)                       | <input type="checkbox"/> Yes            | <input type="checkbox"/> No |
| _____<br>(Number)          | _____<br>(Country) | _____<br>(Day/Month/Year filed)                       | <input type="checkbox"/> Yes            | <input type="checkbox"/> No |

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and insofar as the subject matter of each of the claims of this application is not disclosed in the prior U.S. application in the manner provided by the first paragraph of Title 35, U.S.C. §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

|                                   |                        |   |
|-----------------------------------|------------------------|---|
| _____<br>(Application Serial No.) | _____<br>(Filing Date) | _____<br>(Status: patented, pending, abandoned) |
| _____<br>(Application Serial No.) | _____<br>(Filing Date) | _____<br>(Status: patented, pending, abandoned) |

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

|   |  |                        |
|---|--|------------------------|
| Full Name of First or Sole Inventor<br><u>Gregory J. MOMBER</u>                 | Signature of First or Sole Inventor<br> | Date<br><u>2/20/02</u> |
| Residence Address<br><u>7129 Peach Ridge Road, Grand Rapids, Michigan 49544</u> | Country of Citizenship<br><u>United States of America</u>  |                        |
| Post Office Address<br><u>same as above</u>                                     |  |                        |
| Full Name of Second Inventor (if any)   | Signature of Second Inventor   | Date                   |
| Residence Address   | Country of Citizenship   |                        |
| Post Office Address   |  |                        |
| Full Name of Third Inventor (if any)  | Signature of Third Inventor  | Date                   |
| Residence Address   | Country of Citizenship   |                        |
| Post Office Address   |  |                        |

Docket No.: 357.053/09504754  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:  
Gregory J. Momber

Application No.: 09/913,859

Group Art Unit: N/A

Filed: August 20, 2001

Examiner: Not Yet Assigned

International Filing  
Date: February 18, 2000

For: TRANSFORMERLESS POWER SUPPLY,  
DUAL POSITIVE OR DUAL NEGATIVE  
SUPPLIES

**POWER OF ATTORNEY**

Commissioner for Patents  
Washington, DC 20231

Dear Sir:

ROBERTSHAW CONTROLS COMPANY, assignee of the entire right title and interest in the above-identified application by assignment dated February 20, 2002, submitted herewith, hereby appoints:

Mark Ungerman 32,070 and Lisa Coward 44,091

2

as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that it has reviewed the assignment and to the best of the assignee's knowledge and belief, title is in the assignee.

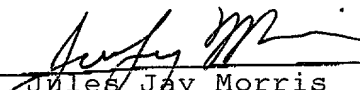
Application No.: 09/913,859

Docket No.: 357.053/09504754

Please direct all correspondence regarding this application to the following:

FULBRIGHT & JAWORSKI L.L.P.  
Attn: Mark E. Ungerman  
Market Square  
801 Pennsylvania Avenue, N.W.  
Washington, DC 20004-2615  
Telephone: (202) 662-0200  
Fax: (202) 662-4643

For: ROBERTSHAW CONTROLS COMPANY

Name:  Dated: 19 MAR 02  
Title: Jules Jay Morris  
Vice President and Chief Intellectual Property Counsel of  
Invensys plc and designated by the Secretary of Robertshaw  
Controls Company to sign on its behalf.

202-662-4643